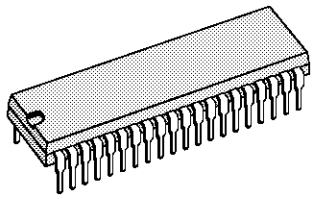
SGS-THOMSON MICROELECTRONICS

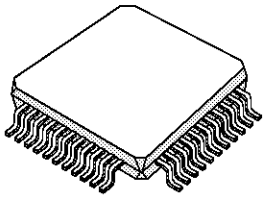
STV3208

8 x 8 DISCRETE COSINE TRANSFORM (DCT)

- 0 TO 27MHz PIXEL RATE IN SINGLE PRECISION MODE,
- 0 TO 20 MHz PIXEL RATE IN DOUBLE PRECISION MODE
- FORWARD AND INVERSE 8 x 8 TRANSFORM
- 9-BIT TWO'S COMPLEMENT PIXEL FORMAT
- 12-BIT TWO'S COMPLEMENT COEFFICIENT FORMAT
- OPTIMIZED ACCURACY FOR 8-BIT TWO'S COMPLEMENT PIXEL FORMAT
- SELECTABLE SCANNING OF COEFFICIENT BLOCKS
- FULLY TTL AND CMOS COMPATIBLE
- CMOS TECHNOLOGY
- SINGLE +5 VOLT POWER SUPPLY
- MAXIMUM POWER DISSIPATION : 750mW AT 27MHz



DIP40
(Plastic Package)



PQFP44
(Plastic Package)

DESCRIPTION

The STV3208 is a dedicated circuit for the 8 x 8 discrete cosine transform (DCT) computation. Two-dimensional forward DCT (FDCT) or inverse DCT (IDCT) is performed for 8 x 8 block sizes and a pixel rate up to 27MHz. The circuit architecture is fully bidirectional with 9-bit magnitude pixel data bus and a 12-bit magnitude coefficient data bus programmed as input or output depending on the selection of FDCT or IDCT.

	FDCT	IDCT	Data Format
Pixel Bus	Input	Output	9-bit 2's Complement
Coefficient Bus	Output	Input	12-bit 2's Complement

For the forward transform, the input pixels are coded on 9-bit 2's complement and the output coefficients are coded on 12-bit 2's complement. For the inverse transform, the data format is identical with the coefficients used as input and the pixels used as output.

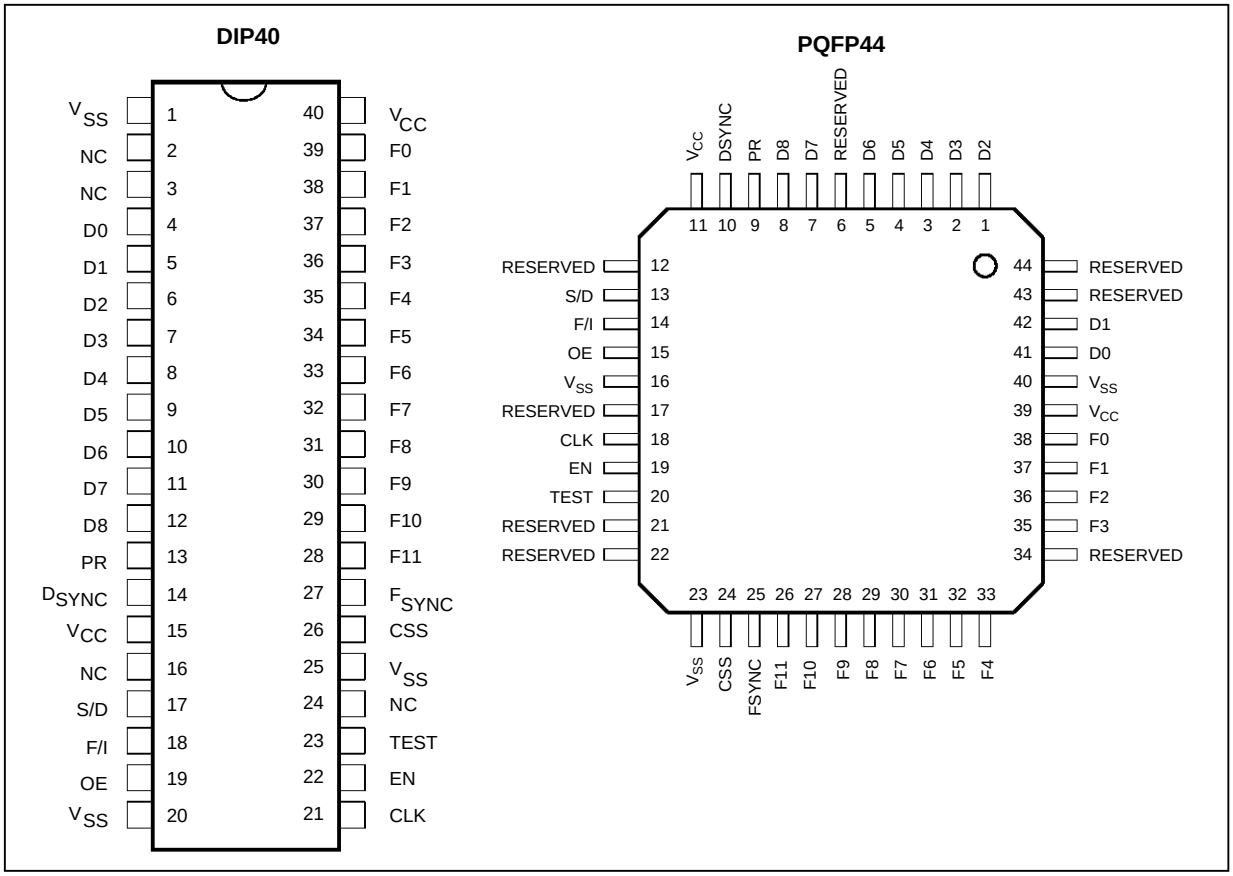
Two operating modes are provided : single precision mode at a pixel rate up to 27 MHz, and double precision mode at a pixel rate up to 20 MHz.

ORDER CODES

Part Number	Temperature Range	Package
STV3200CP	0 to 70°C	DIP 40
STV3200CV	0 to 70°C	PQFP44

3208-01.TBL

PIN CONNECTIONS



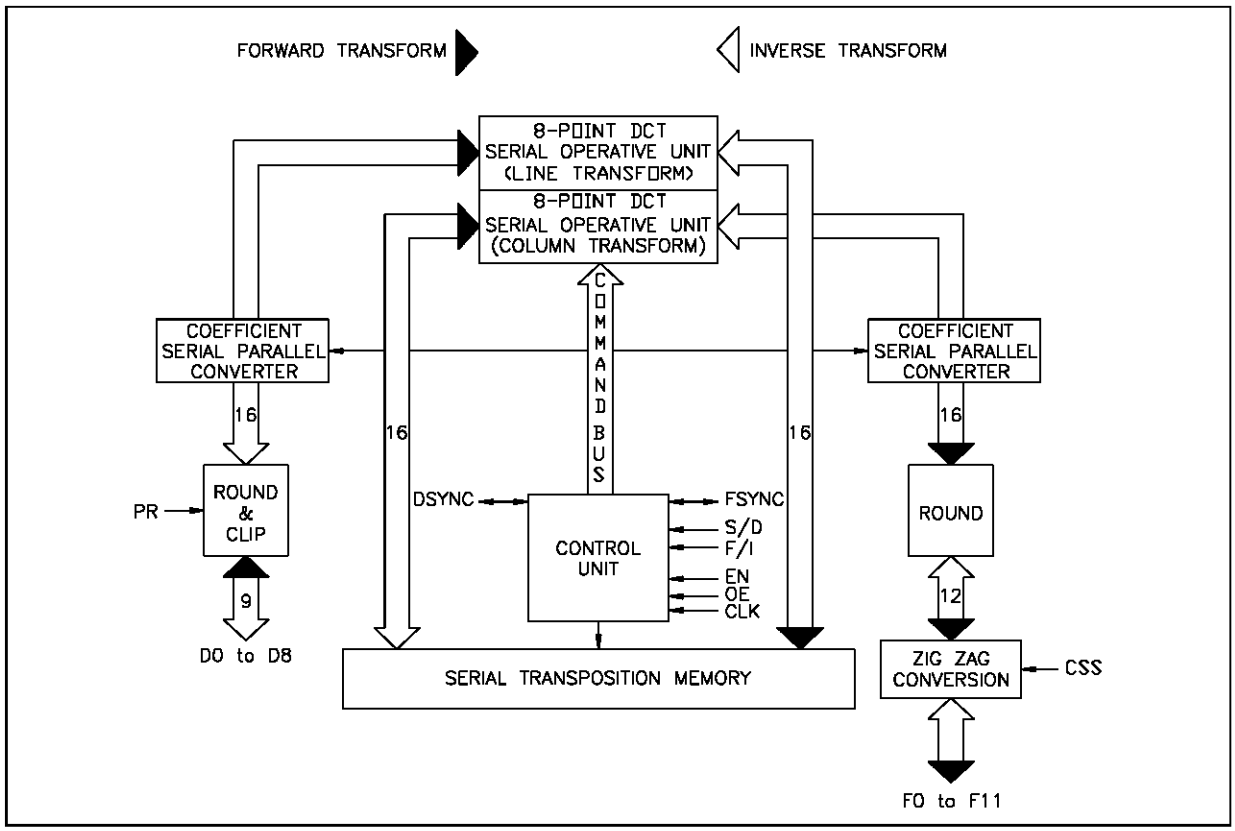
3208-01A.EPS / 3208-01B.EPS

PIN IDENTIFICATION

Pin Number	Symbol	Type	Function / Description
4-12	D0 to D8	I/O	Pixel data bus
13	PR	Input	Pixel range selection
14	DSYNC	I/O	Pixel block synchronization signal
17	S/D	Input	Single/double precision selection
18	F/I	Input	FDCT/IDCT selection
19	OE	Input	Output three-state control
21	CLK	Input	Clock signal
22	EN	Input	Clock enable signal
23	TEST	Input	Test mode selection
26	CSS	Input	Zig Zag selection
27	FSYNC	I/O	Coefficient block synchronization signal
28-39	F0 to F11	I/O	Coefficient data bus
1,20,25	VSS	Power	Ground
15,40	VCC	Power	Power supply
2,3,24	NC		Not Connected

3208-02.TBL

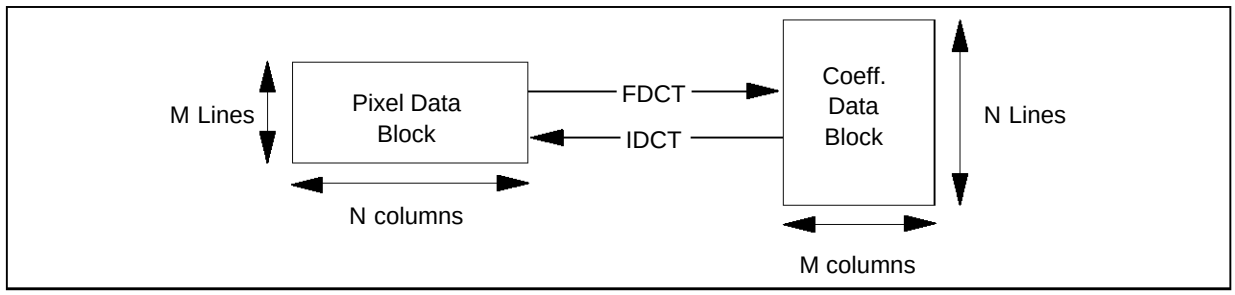
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1. EQUATIONS

Figure 1



The STV3208 performs 8 x 8 two dimensional Discrete Cosine Transform according to the following formula:

Equations for 9-bit PIXEL DATA (PR pin set to low) :

FORWARD TRANSFORM EQUATION :

$$F(u,v) = \text{Round}\left[\frac{1}{4}C(u)\,C(v)\sum_{i=0}^{7}\sum_{j=0}^{7}D(i,j)\,\cos\frac{(2\cdot i+1)\,u\,\pi}{16}\,\cos\frac{(2\cdot j+1)\,v\,\pi}{16}\right]$$

INVERSE TRANSFORM EQUATION :

$$D(i,j) = \text{Round}\left[\frac{1}{4}\sum_{u=0}^{7}\sum_{v=0}^{7} C(u)\ C(v)\ F(u,v)\ \cos\frac{(2\cdot i+1)\ u\pi}{16}\ \cos\frac{(2\cdot j+1)\ v\pi}{16}\right]$$

Where $C(u) = \frac{1}{\sqrt{2}}$ if $u = 0$

$= 1$ otherwise

Equations for 8-bit PIXEL DATA (PR pin set to high) :

FORWARD TRANSFORM EQUATION :

$$F(u,v) = \text{Round}\left[\frac{1}{2}C(u)\,C(v)\sum_{i=0}^{7}\sum_{j=0}^{7} D(i,j)\ \cos\frac{(2\cdot i+1)\ u\,\pi}{16}\ \cos\frac{(2\cdot j+1)\ v\,\pi}{16}\right]$$

INVERSE TRANSFORM EQUATION :

$$D(i,j) = \text{Round}\left[\frac{1}{8}\sum_{u=0}^{7}\sum_{v=0}^{7} C(u)\ C(v)\ F(u,v)\ \cos\frac{(2\cdot i+1)\ u\pi}{16}\ \cos\frac{(2\cdot j+1)\ v\pi}{16}\right]$$

Where $C(u) = \frac{1}{\sqrt{2}}$ if $u = 0$

$= 1$ otherwise

2. DATA FLOW ORDERING

The pixel block is scanned column by column (ORDER 1) or line by line (ORDER 2). If CSS is high, the coefficient block is scanned with a zig zag order. Figure 2 shows the relation between pixels order and coefficient order.

Figure 2a : Data Ordering (CSS high)

	PIXEL ORDER									COEFFICIENT ORDER							
ORDER 1	1	9	17	25	33	41	49	57	⇔	1	2	6	7	15	16	28	29
	2	10	18	26	34	42	50	58		3	5	8	14	17	27	30	43
	3	11	19	27	35	43	51	59		4	9	13	18	26	31	42	44
	4	12	20	28	36	44	52	60		10	12	19	25	32	41	45	54
	5	13	21	29	37	45	53	61		11	20	24	33	40	46	53	55
	6	14	22	30	38	46	54	62		21	23	34	39	47	52	56	61
	7	15	23	31	39	47	55	63		22	35	38	48	51	57	60	62
	8	16	24	32	40	48	56	64		36	37	49	50	58	59	63	64
ORDER 2	1	2	3	4	5	6	7	8	⇔	1	3	4	10	11	21	22	36
	9	10	11	12	13	14	15	16		2	5	9	12	20	23	35	37
	17	18	19	20	21	22	23	24		6	8	13	19	24	34	38	49
	25	26	27	28	29	30	31	32		7	14	18	25	33	39	48	50
	33	34	35	36	37	38	39	40		15	17	26	32	40	47	51	58
	41	42	43	44	45	46	47	48		16	27	31	41	46	52	57	59
	49	50	51	52	53	54	55	56		28	30	42	45	53	56	60	63
	57	58	59	60	61	62	63	64		29	43	44	54	55	61	62	64

3208-03.TBL

If CSS is low, the coefficient block is scanned line by line and the pixel block is scanned column by column, or the coefficient block is scanned column by column and the pixel block is scanned line by line.

Figure 2b : Data Ordering (CSS low)

	PIXEL ORDER									COEFFICIENT ORDER							
ORDER 1	1	9	17	25	33	41	49	57	⇔	1	2	3	4	5	6	7	8
	2	10	18	26	34	42	50	58		9	10	11	12	13	14	15	16
	3	11	19	27	35	43	51	59		17	18	19	20	21	22	23	24
	4	12	20	28	36	44	52	60		25	26	27	28	29	30	31	32
	5	13	21	29	37	45	53	61		33	34	35	36	37	38	39	40
	6	14	22	30	38	46	54	62		41	42	43	44	45	46	47	48
	7	15	23	31	39	47	55	63		49	50	51	52	53	54	55	56
	8	16	24	32	40	48	56	64		57	58	59	60	61	62	63	64
ORDER 2	1	2	3	4	5	6	7	8	⇔	1	9	17	25	33	41	49	57
	9	10	11	12	13	14	15	16		2	10	18	26	34	42	50	58
	17	18	19	20	21	22	23	24		3	11	19	27	35	43	51	59
	25	26	27	28	29	30	31	32		4	12	20	28	36	44	52	60
	33	34	35	36	37	38	39	40		5	13	21	29	37	45	53	61
	41	42	43	44	45	46	47	48		6	14	22	30	38	46	54	62
	49	50	51	52	53	54	55	56		7	15	23	31	39	47	55	63
	57	58	59	60	61	62	63	64		8	16	24	32	40	48	56	64

3208-04.TBL

3. DATA FORMAT

Coefficients format is 12-bit 2's complement, corresponding to the range -2048 to 2047.

There are 2 possible ranges for pixel data :

9-bit two's complement magnitude
(see Figure 3)

The pixel data range is -256 to +255. In this case the PR pin must be set to 0 for IDCT. D8 is the most significant bit and D0 the least significant bit for the pixel data. A clipping to the range -256 to +255 is performed before outputting reconstructed pixels after an IDCT.

8-bit two's complement magnitude
(see Figure 4)

Pixel data range is -128 to +127. In this case D0 must be set to 0 and the PR Pin must be set to 1 for IDCT. D8 is the most significant bit and D1 the least significant bit for the pixel data. A clipping to the range -128 to +127 is performed before outputting reconstructed pixels after an IDCT.

This mode may be used for intra picture coding. In this case, pixel data range is 0 to 255. For a FDCT, the most significant bit of input pixel data (D8) must be inverted before entering the chip. This is equivalent to substract 128 to the input pixel data. Note that this operation will only have effect on the DC value F(0,0). For an IDCT, the most significant bit of output pixel data (D8) must be inverted. This is equivalent to add 128 to the output pixel data.

Figure 3

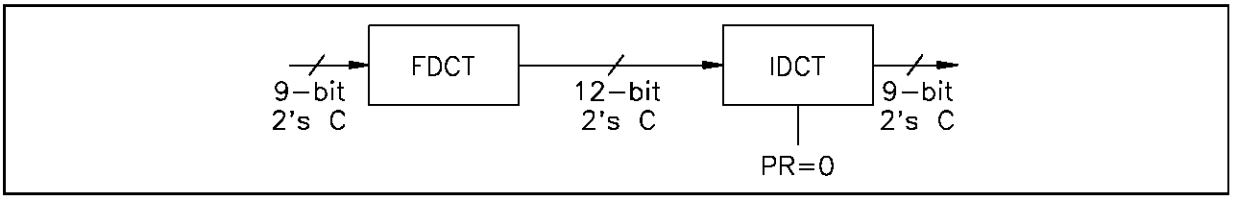


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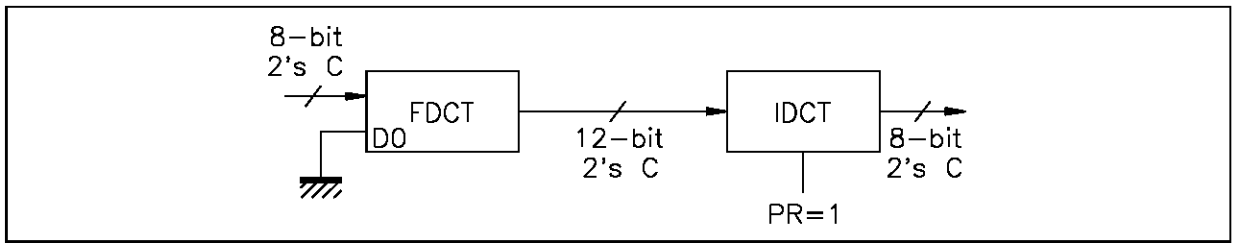
Figure 4



4. BLOCK FLOW

Depending on the application, blocks may be entered in different way.

Latent period :

The latent period between input data and corresponding output results is 167 clock cycles (if FDCT is selected) or 163 clock cycles (if IDCT is selected) in single precision mode (S/D pin set to 1). This means that the first data of the resulting block is provided 137 clock cycles (if FDCT is selected) or 135 clock cycles (if IDCT is selected) in double precision mode (S/D pin set

to 0).

Latency	Forward DCT	Inverse DCT
S/D = 1 Single Precision	167 Cycles	163 Cycles
S/D = 0 Double Precision	137 Cycles	135 Cycles

Synchronization signals :

An input block synchronization signal must be provided. The input pin for this signal is DSYNC if FDCT is selected and FSYNC if IDCT is selected.This signal is active low and must not be active more than one clock cycle and during the first clock cycle after power-up.This signal must be active with the first data of each input block or group of blocks.

An output block synchronization signal is provided. The output pin for this signal is FSYNC if FDCT is selected and DSYNC if IDCT is selected. This signal is active with the first data of each output block or group of blocks.

The output synchronization signal is equal to the input synchronization signal delayed from the latent period (see Figure 5).

CONTINUOUS BLOCK FLOW

Inputs data are fed continously with one new item data at each clock cycle and output data is provided continously with one new result data item at each clock cycle.

The input synchronization signal can be provided for each input block. In this case the output synchronization pulse is provided for each output block (Figure 6). An other way is to provide a synchronization pulse only for the first block of a group of blocks. In this case, only one synchronization pulse is provided for the first output block (Figure 7).

Figure 5

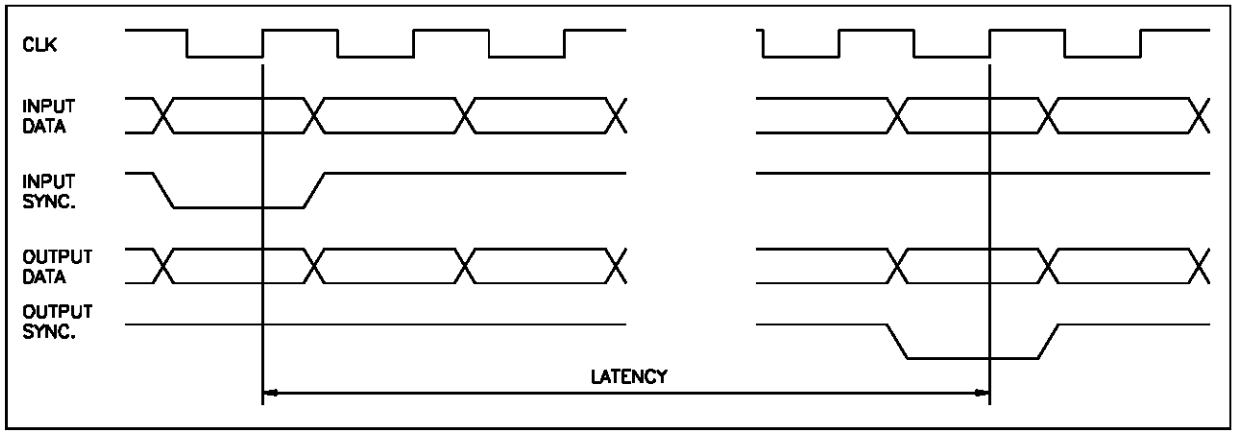


Figure 6 : Continuous Block Flow 1

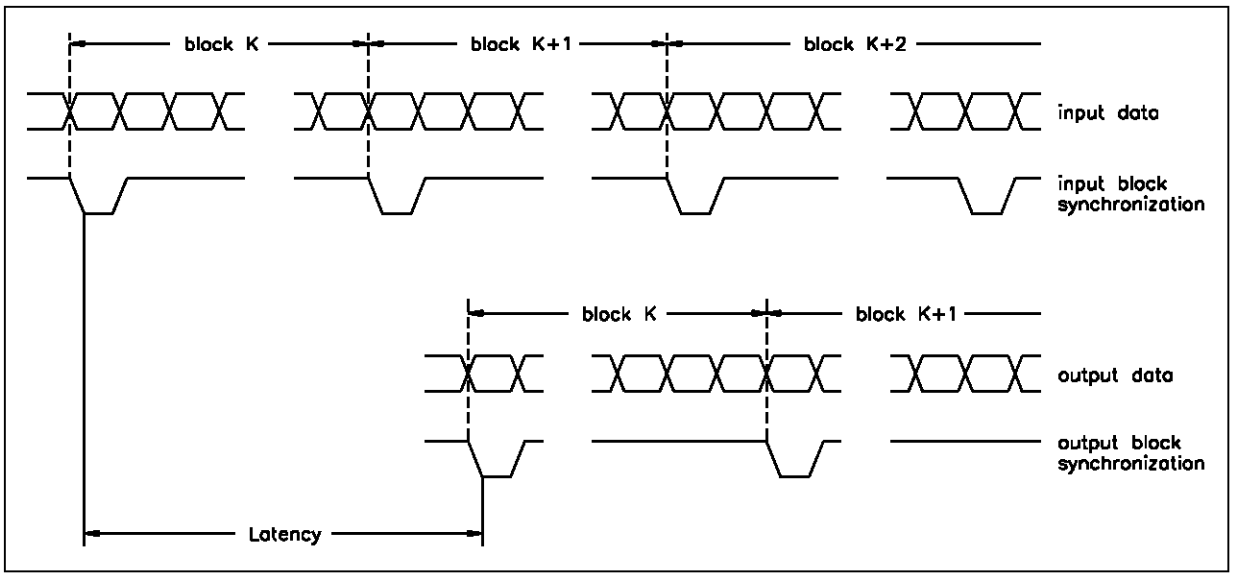
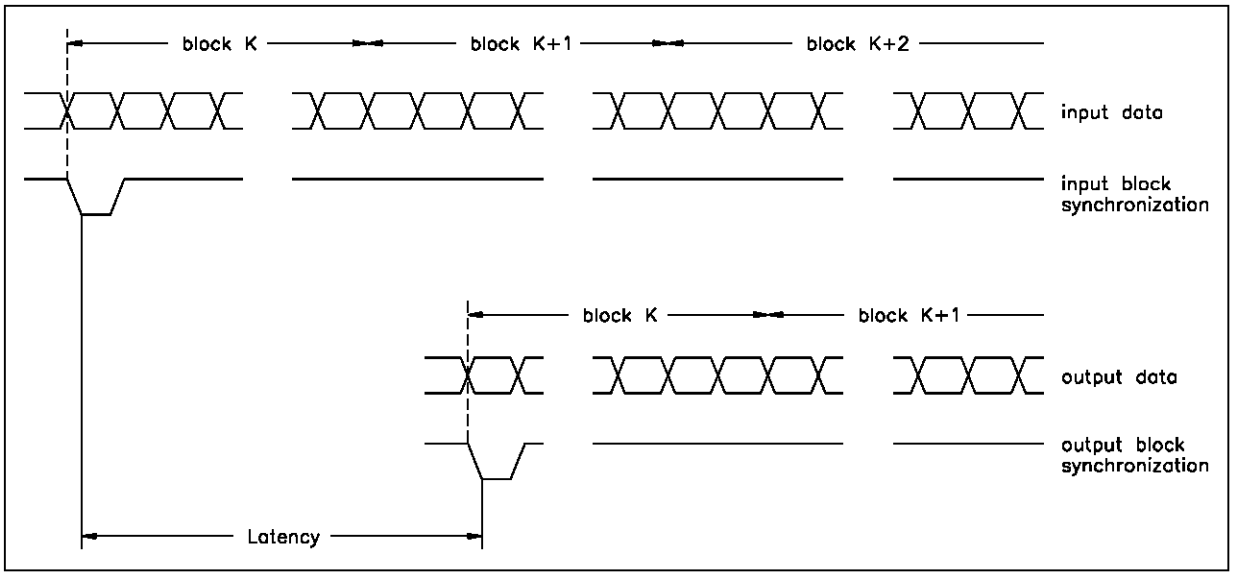


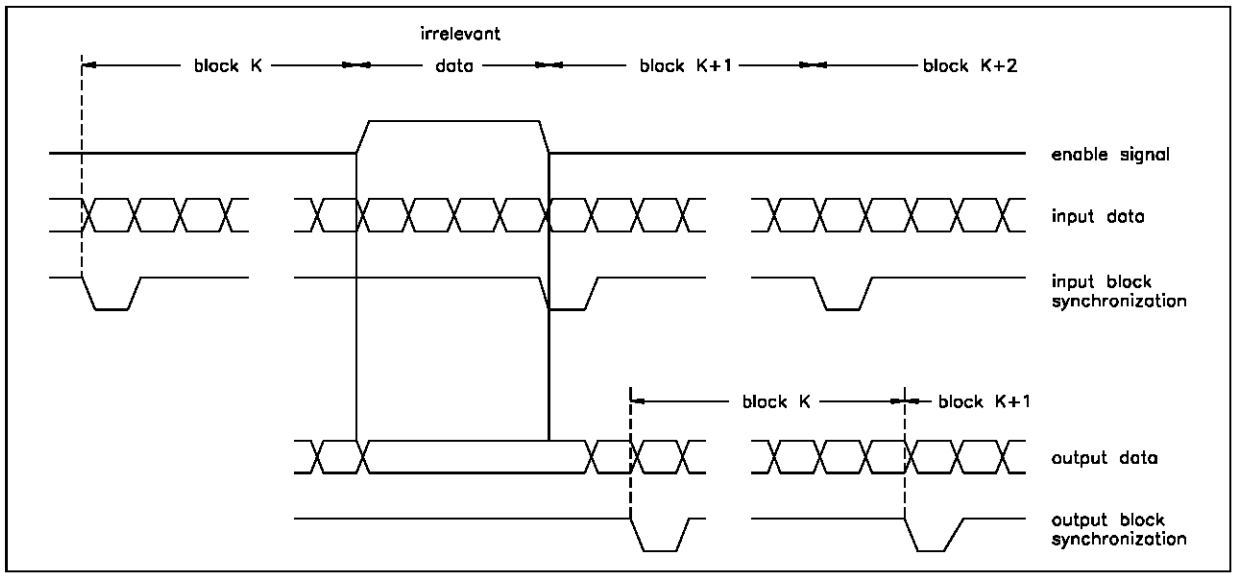
Figure 7 : Continuous Block Flow 2



CONTINUOUS BLOCK FLOW WITH BYPASS OF IRREVELANT DATA

It is possible to process a block flow including irrelevant data (corresponding to line suppression for example) as if it was a continous block flow. One way is to stop the clock signal during the irrelevant data occurence. Another way is to use the Clock Enable Signal (EN) which allows to stop the chip internal clock during irrelevant data occurrence (see Figure 8)

Figure 8 : Continuous Block Flow with Irrelevant Data



BURST BLOCK FLOW (see Figure 9)

Single blocks (or groups of block) may not be continous. In other words, delay cycles between two blocks (or groups of block) may exist. During these delay cycles, the clock is still running and the chip continues to perform computations. The constraint is that the internal pipe line must not be broken when the new block occurs.To take this constraint into account, the number of delay cycles (NC) must respect one of the following conditions :

1 - the number of delay cycles (NC) is greater than or equal to the latency. In this case the pipe line is empty (all the relevant data has been output) when a new input block processing starts.

2 - the number of delay cycles (NC) is a multiple of 64. In this case, the input data always remains synchronous with the internal pipe line.

MIXED FDCT/IDCT (see Figure 10)

In some low frequency application, it could be cost effective to use only one chip to compute all the DCT required by the coding scheme. Blocks must be fed in a burst fashion with at least the latency time between the last pixel of input pixels for FDCT and the first pixel of input coefficients for IDCT. The same delay must be respected between the last pixel of input coefficients for IDCT and the first pixel of input pixels for FDCT.

Figure 9 : Burst Block Flow

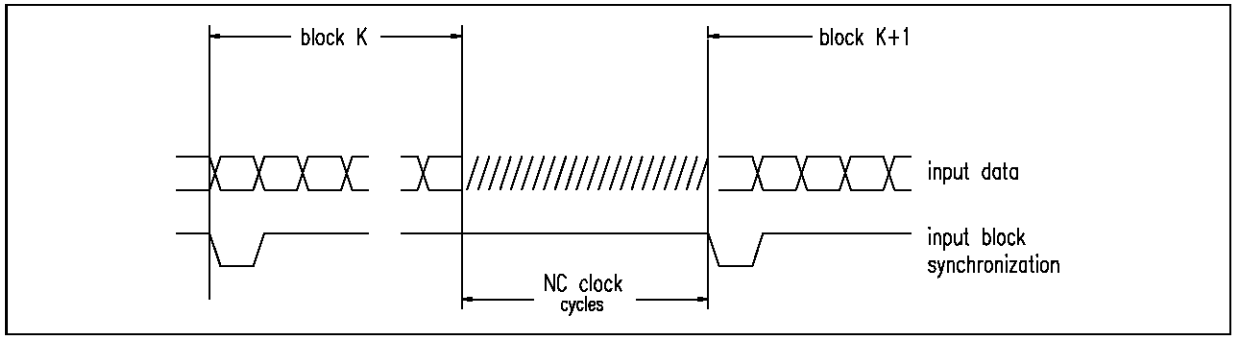
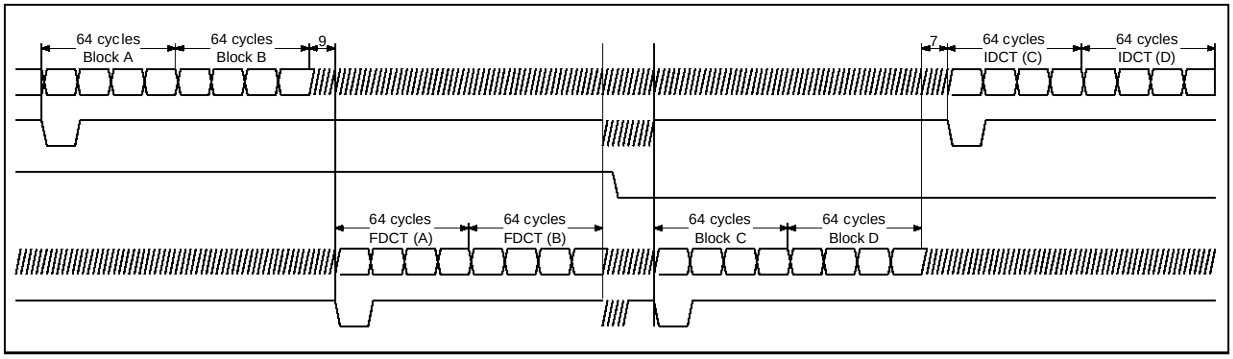


Figure 10 : Mixed 8 x 8 FDCT/IDCT Example Waveforms (double precision)



PRECISION SELECTION

For single precision mode, the S/D pin must be high. In this case, the maximum rating for pixel is 27 MHz. For double precision mode, the S/D pin must be low. In this case, the maximum rating for pixel is 20 MHz.

5. PINS DESCRIPTION

CLK : Clock signal

DATA PINS

D0 to D8 : 9-bit bidirectional pixel data bus pins. Direction is programmed by the F/I pin :

F/I state	D0 to D8 Direction
High	Input
Low	Output

Data is loaded (when input) or settled (when output) on rising edge of CLK. D0 is the least significant bit and D8 the most significant one. Note that for the optimized mode for 8-bit 2's C pixel data, D1 is the least significant bit and D0 must be set to 0.

MSB								LSB	
D8	D7	D6	D5	D4	D3	D2	D1	D0	Pin
-256	128	64	32	16	8	4	2	1	Weight

DSYNC : pixel data block synchronization signal. This pin is bidirectional with the direction programmed by the F/I pin (like D0 to D8). DSYNC is active (low level during one clock cycle only) with the first pixel data of a block (or a group of blocks).

F0 to F11 : 12-bit bidirectional coefficient data bus pins. Direction is programmed by the F/I pin :

F/I state	F0 to F11 direction
High	Output
Low	Input

Data is loaded (when input) or settled (when output) on rising edge of CLK. F0 is the least significant bit and F11 the most significant one.

MSB											LSB	
F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	Pin
-2048	1024	512	256	128	64	32	16	8	4	2	1	Weight

FSYNC : coefficient data block synchronization signal. This pin is bidirectional with the direction programmed by the F/I pin (like F0 to F11). FSYNC is active (low level during one clock cycle only) with the first coefficient data of a block (or a group of blocks).

CONTROL PINS

F/I : forward or inverse selection. When F/I is high, forward DCT is performed, when F/I is low, inverse DCT is performed.

S/D : single or double precision. When S/D is high, single precision is selected. When S/D is low, double precision is selected.

CSS : coefficient scanning selection. When CSS is high, zig zag scanning of coefficient block is selected. When CSS is low, row scanning of coefficient block is selected.

PR : pixel range selection. If PR is low, pixel range is -256 to +255. If PR is high, pixel range is -128 to +127.

OE : output enable. This signal is active low. When OE is high, all outputs (defined by the F/I pin state) are forced to the high impedance state.

EN : enable. This signal is active low. When EN is high, internal states of the chip are frozen. When EN becomes low, execution restarts. EN must go to high state when CLK is high.

State	Function
F/I is High F/I is Low	Forward DCT Inverse DCT
S/D is High S/D is Low	Single Precision Double Precision
CSS is High CSS is Low	Zig Zag Scanning of coefficients Row Scanning of coefficients
PR is High PR is Low	8-bit 2's C Pixel Data 9-bit 2's C Pixel Data
OE is High OE is Low	High Impedance Outputs Outputs Active
EN is High EN is Low	Internal Clock is stopped Internal Clock runs

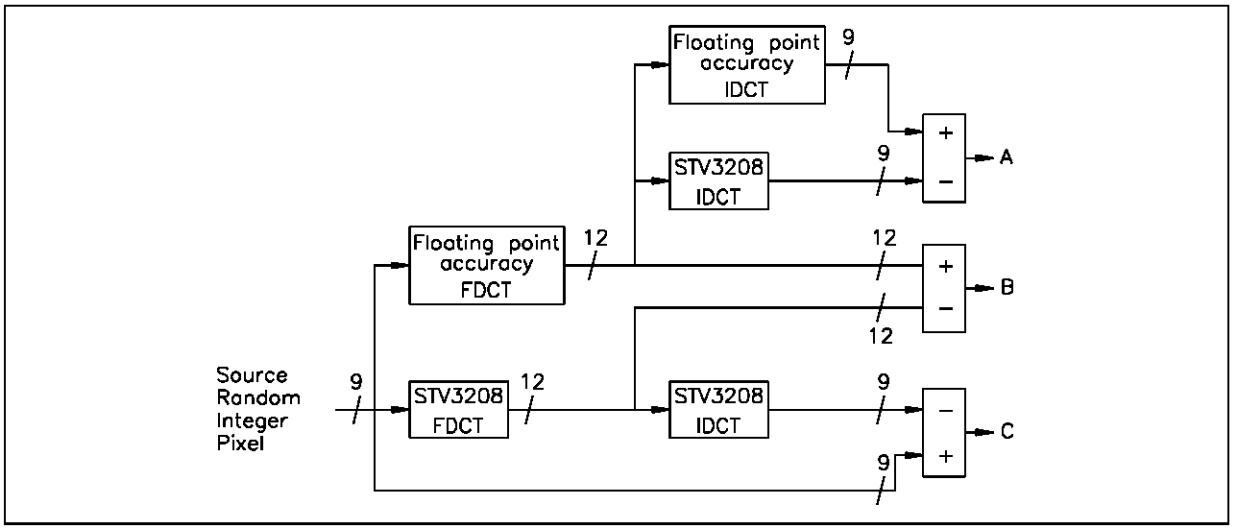
POWER SUPPLY AND GROUND PINS

V_{CC} : +5 Volt power supply
V_{SS} : ground potential

OTHERS : Test. This pin is reserved and must be low in normal mode.

6. ACCURACY CHARACTERISTICS

The accuracy characteristics have been measured according to the following scheme :



A :

Characteristics of IDCT. Error between the IDCT computed with 64-bit floating point accuracy and the IDCT computed by the STV3208 is measured. Measures have been done according to the CCITT WGXV method

	Single Precision	Double Precision
Peak Error	1	1
Peak Mean Square Error	0.0403	0.0258
Overall Mean Square Error	0.0287	0.0200
Peak Mean Error	0.0125	0.0041
Overall Mean Error	0.0050	0.0000062

	9-bit pixels		8-bit pixels	
	Single Precision	Double Precision	Single Precision	Double Precision
Exact value	97.1 %	98.0 %	99.96 %	99.97 %
Errors of ± 1 LSB	2.9 %	2.0 %	0.04 %	0.03 %
Errors of ± 2 LSB	0 %	0 %	0 %	0 %

B :

Characteristics of FDCT. Error between the FDCT computed with 64-bit floating point accuracy and the FDCT computed by the STV3208 is measured.

	9-bit pixels		8-bit pixels	
	Single Precision	Double Precision	Single Precision	Double Precision
Exact value	93.6 %	96.9 %	93.6 %	96.9 %
Errors of ± 1 LSB	6.4 %	4.1 %	6.4 %	4.1 %
Errors of ± 2 LSB	0 %	0 %	0 %	0 %

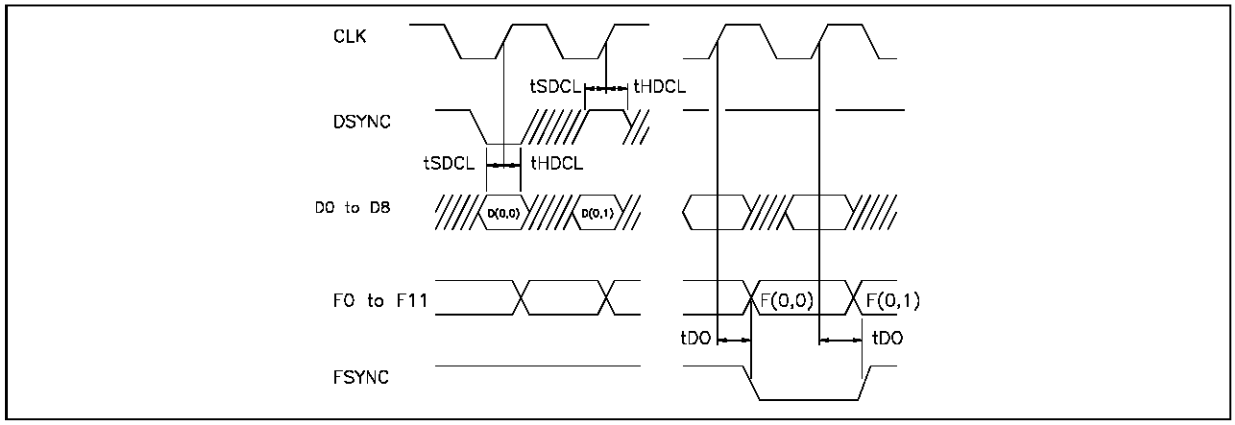
C :

Characteristics of FDCT followed by an IDCT. Error between the source picture and the FDCT computed by the STV3208 followed by an IDCT computed by the STV3208 is measured.

	9-bit pixels		8-bit pixels	
	Single Precision	Double Precision	Single Precision	Double Precision
Exact value	89.3 %	90.6 %	99.88 %	99.92 %
Errors of ± 1 LSB	10.7 %	9.4 %	0.12 %	0.08 %
Errors of ± 2 LSB	0 %	0 %	0 %	0 %

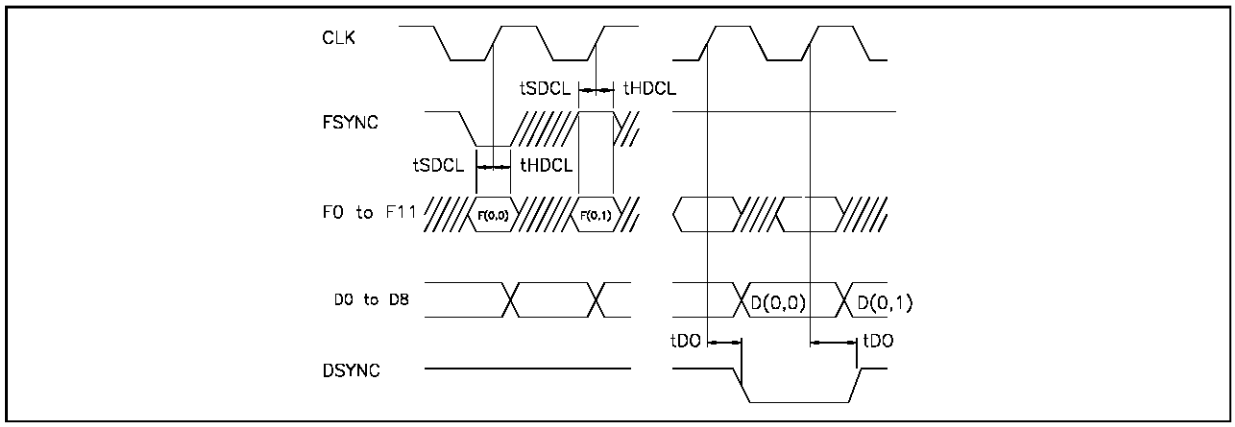
TIMING WAVEFORMS

Synchonization Signals Timing Diagram for a Forward Transform



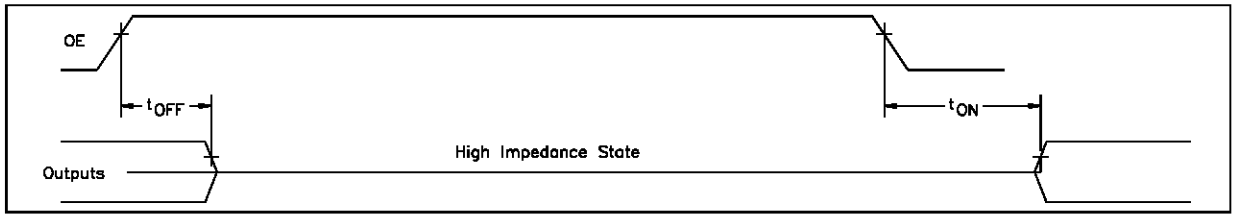
Note : FSYNC will be in unknown state after the power up during a count of cycles equal to the latency.

Synchronization Signals Timing Diagram for an Inverse Transform

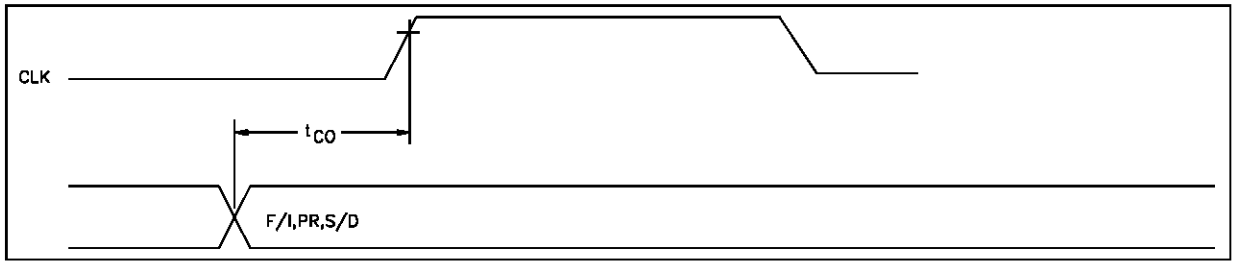


Note : DSYNC will be in unknown state after the power up during a count of cycles equal to the latency.

Output Enable Signal Timing Waveforms

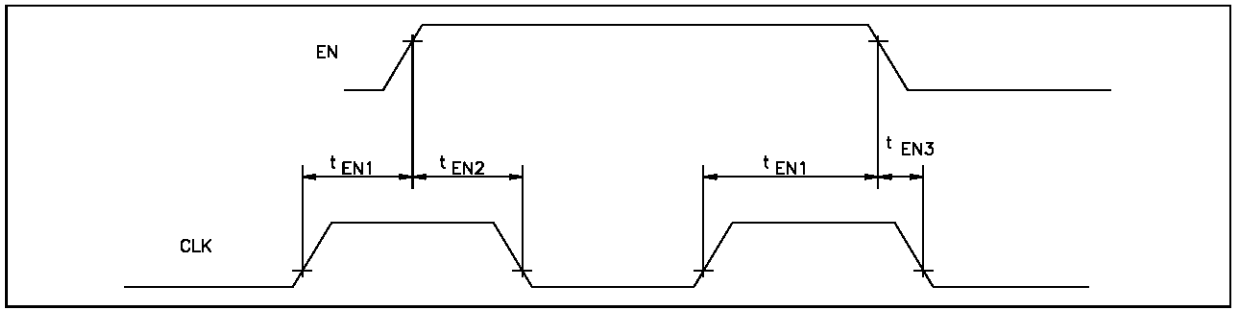


Control Static Signal Timing Waveforms



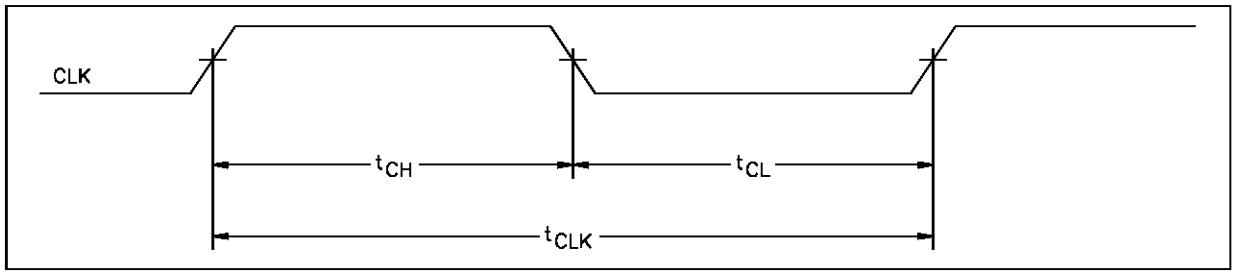
TIMING WAVEFORMS (continued)

Enable Signal Timing Waveforms

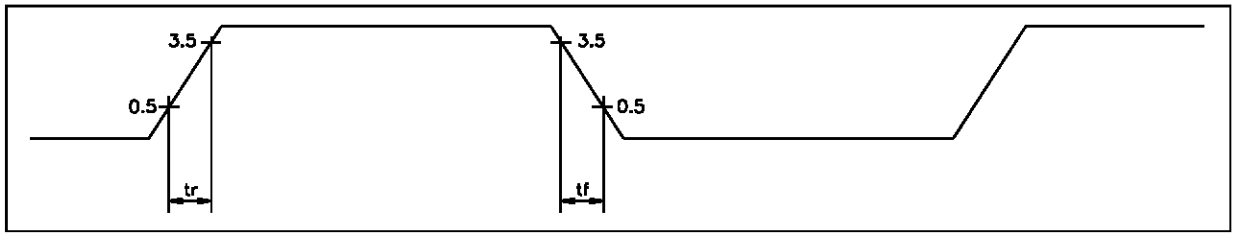


Note : EN signal must change from low to high level during the high level of CLK signal.

Clock Timing Waveforms



Output Timing Waveforms



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC}) : 6 Volts
Operating temperature range : 0 to 70 °C

DC ELECTRICAL CHARACTERISTICS

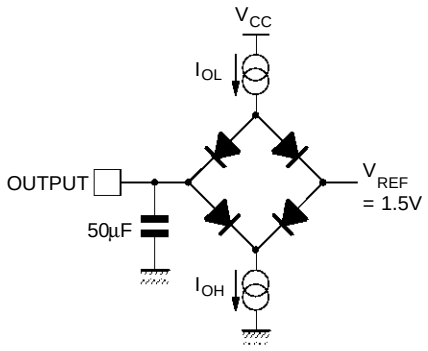
Operating Conditions : V_{SS} = 0 Volt, T_A = 0 to 70 °C, V_{CC} = 5 V ± 5% unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.75		5.25	V
I_{CC}	Supply current : F_{CLK} = 27 MHz F_{CLK} = 0 MHz	C_{LOAD} = 50 pF on all outputs. All inputs at V_{CC} or V_{SS}			 150 1	 mA mA
V_{IL} V_{IH}	Input Voltage Level (except CLK) Logic Low Logic High	V_{CC} = 5 ± 0.25 V	 2		0.8	V V
$V_{IL(CLK)}$ $V_{IH(CLK)}$	Clock Signal Logic Low Logic High		 2.5		0.5	V V
	High Impedance input leakage : I/O Buffers Input Buffers	V_{IN} = V_{SS} to V_{CC}	 -5 -1		 +5 +1	 µA µA
V_{OL} V_{OH}	Output Voltage Level : Logic Low I_{LOAD} = 500µA Logic High I_{LOAD} = -500µA	V_{CC} = 4.75 V	 2.7		0.4	V V
C_{IN}	Input capacitance	V_{OFFSET} = 2.5 V, f = 1 MHz			10	pF

3208-05.TBL

AC ELECTRICAL CHARACTERISTICS

Operating conditions : V_{SS} = 0 Volt, T_A = 0 to 70 °C, V_{CC} = 5 V ± 5 % unless otherwise specified
Outputs Loads : Capacitance = 50 pF, Current Logic Low = 500µA
Test Load on Outputs :



3208-20.EPS

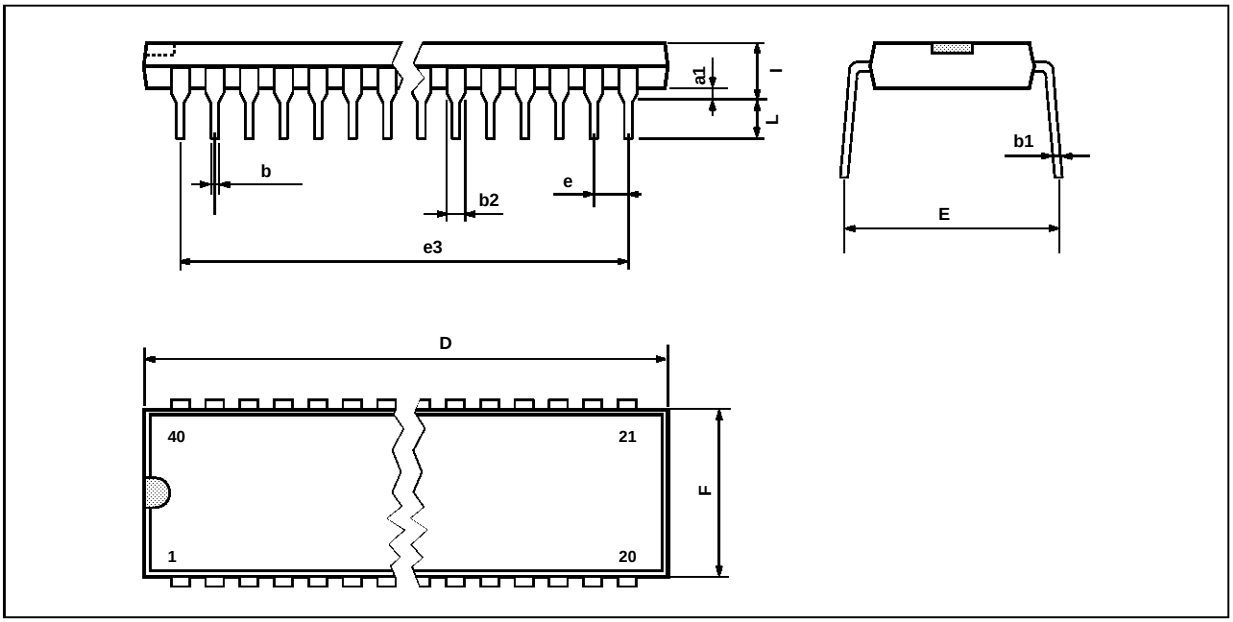
Timings are measured between threshold voltage of 1.5 V unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_R	Rising time from 0.5 to 3.5 V			10	ns
t_F	Falling time from 3.5 to 0.5 V			10	ns
t_{CH}	Clock High Pulse Width S/D = 1 S/D = 0	 15 24			 ns ns
t_{CL}	Clock Low Pulse Width S/D = 1 S/D = 0	 15 24			 ns ns
t_{CLK}	Clock Cycle Duration S/D = 1 S/D = 0	 37 50			 ns ns
t_{SDCL}	Data Setup Time from CLK ↑	8			ns
t_{HDCL}	Data Hold Time from CLK ↑	0			ns
t_{DO}	Output Data Delay from CLK ↑			15	ns
t_{EN1}	Enable Hold Time from CLK ↑	0			ns
t_{EN2}	Enable Rising Edge Setup Time from CLK ↓	5			ns
t_{EN3}	Enable Falling Edge Setup Time from CLK ↓ S/D = 1 S/D = 0	 0 0			 ns ns
t_{OFF}	Delay from OE ↑ to Output going to High Impedance State			15	ns
t_{ON}	Delay from OE ↓ to Output going to High or Low State			15	ns
t_{CO}	F/I , CSS, PR, S/D Setup Time from Beginning of Input Stream	100			ns

3208-06.TBL

PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



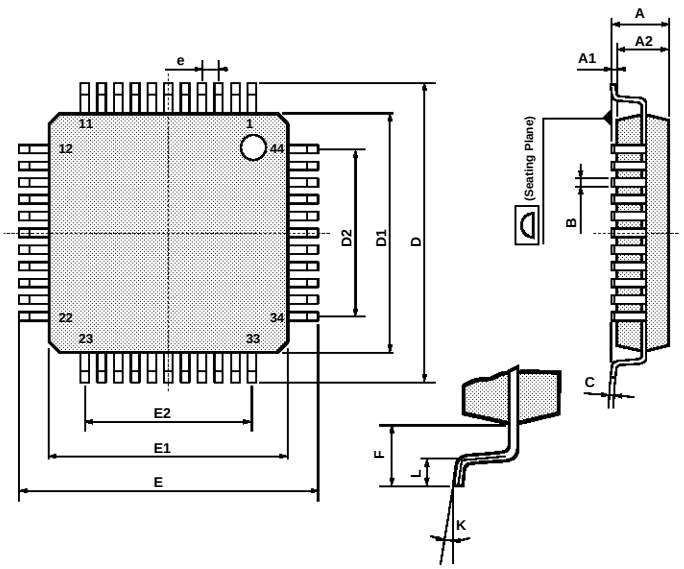
PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL

PACKAGE MECHANICAL DATA

44 PINS - PLASTIC QUAD FLAT PACK



PMPQFP44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.35		0.50	0.014		0.020
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

PQFP44.TBL